

TRANSISTOR GATE AND LOCAL INTERCONNECTRelated Applications

5 This application is a divisional of U.S. Patent Application No. 09/360,703 filed July 26, 1999 and which is incorporated herein in its entirety by reference.

Background of the InventionField of the Invention

10 The present invention relates to semiconductor integrated circuit fabrication, devices and methods, and, in particular, is directed toward the method of forming a unique silicide local interconnect structure that extends from an exhumed gate electrode.

Description of the Related Art

15 As is well known in the semiconductor processing industry, refractory silicides are often used to form local interconnects between circuit nodes in a semiconductor integrated circuit. In particular, when a refractory metal, for example titanium (Ti), is deposited flushly adjacent a silicon material and exposed to a sufficiently high temperature, the refractory metal will react with the silicon material to form a refractory silicide contact, for example titanium silicide (TiSi_2). Since the resulting silicide contact has a relatively low sheet resistance, interconnects having silicide contacts can
20 be formed with a reduced size, thereby enabling increased circuit density.

 While silicides are very versatile as materials for forming interconnecting structures in integrated circuits, in some applications the silicides may poorly interconnect to particular semiconductor devices. For example, with some exhumed contact structures, the processing steps may result in the interconnect structure being
25 undercut at an exposed region adjacent the exhumed contact which can result in either a higher resistance contact or an open contact which may be inadequate for a particular application.

 For example, Fig. 1 illustrates a known exemplary method of forming a silicide local interconnect 200 in a typical semiconductor device. In particular, the device
30 comprises a plurality of gate stacks 204 that are preformed with a gate oxide layer 212 deposited on a substrate 208, a polysilicon layer 214 deposited on the gate oxide layer

212, a laterally conducting tungsten silicide (WSix) layer 210 deposited on the polysilicon layer 214, and an insulating layer 216 deposited over the tungsten silicide layer 210.

In this example, the local interconnect 200 extends between an exhumed surface 202 of the gate stack 204a and a distally positioned active region 206 of the substrate 208. In particular, the exhumed surface 202 corresponds to the upper surface of the laterally conductive tungsten silicide layer 210 of the gate stack 204a and the active region 206 of the substrate 208 corresponds to a source/drain surface region of an isolated CMOS transistor.

To form the interconnect 200, a layer of refractory metal, such as titanium (Ti) 218 is deposited above the silicon substrate 208 so that the refractory metal layer 218 contacts both the exhumed surface 202 of the gate stack 204a and the active region 206 of the substrate 208. A masking layer 220 is then deposited over the refractory metal layer 218 and etched so as to define the extent of the local interconnect 200. The masking layer 220, which may comprise silicon, polysilicon, silicon rich tungsten silicide, or silicon oxynitride, also acts as a source of silicon to promote silicide formation along the length of the interconnect 200 during a subsequent annealing process. The device then undergoes the well-known high temperature annealing process which transforms the refractory metal into a silicide, such as titanium silicide (TiSi_2), at the active region 206 of the substrate 208 and at the exhumed surface 202 of the gate stack 204a. The transformation of the refractory material into a silicide at these locations results in a desirable low resistance contact between the exhumed contact, the active area and the interconnect. Subsequently, a selective wet etching process is then used to remove exposed excess refractory metal and other exposed refractory metal byproducts. Thus, the remaining refractory material positioned underneath the masking layer 220 forms the local interconnect 200 having titanium silicide contacts 222 and 224 formed at the exhumed surface 202 of the gate stack 204a and active region 206 of the substrate 208 respectively.

However, Fig. 1 illustrates a common problem associated with this kind of interconnect. In particular, since the exhumed tungsten silicide surface 202 is often a relatively poor source of silicon and since the width of the exhumed surface 202 is often

relatively small, an underproduction of titanium silicide during annealing at the exhumed surface 202 often results. Thus, the selective wet etching process often results in the silicide contact 222 having a very severe undercut 226, as shown in Fig. 1. Consequently, the resistance of the titanium silicide contact 222 formed at the exhumed surface 202 of the gate stack 204a may be relatively large. Thus, circuit performance may be compromised and production yields may be decreased. Moreover, such problematic local interconnects may limit the extent of selective wet cleans, which could impede the development of increasingly reduced circuit dimensions.

From the foregoing, it will be appreciated that there is a need for an improved method of forming local interconnects that extend from an exhumed surface of a gate stack. In particular, there is a need for an improved method that results in the contact formed at the exhumed surface of the gate stack having a decreased resistance. To this end, there is a need for the local interconnect to be formed such that undercutting of the material at the exhumed surface of the gate stack is substantially reduced. Furthermore, there is a need for such a local interconnect to be formed in a simple and, therefore, cost effective manner.

Summary of the Invention

The aforementioned needs are satisfied by the integrated circuit of the present invention. According to one aspect of the invention, the integrated circuit comprises a semiconductor substrate and a first electrical structure formed in the semiconductor substrate. The integrated circuit further comprises a gate stack formed on the semiconductor substrate, the gate stack having at least one conductive layer and a source layer positioned on the conductive layer. The integrated circuit further comprises a local interconnect interconnecting the conductive layer of the gate stack to the first electrical structure. In particular, the local interconnect is attached to the gate stack at an exhumed surface adjacent the layer of source material. Moreover, the local interconnect includes a conductive material to provide a low resistance contact with the first electrical structure formed in the semiconductor substrate. The source layer provides transforming atoms to the material used to form the local interconnect during formation such that the density of dopant atoms in the material used to form the local interconnect during formation is

sufficient to substantially prevent undercutting of the local interconnect at the connection to the gate stack.

5 In one embodiment, the conductive material used to form the local interconnect comprises a refractory metal. In this embodiment, the refractory metal preferably comprises titanium and the source layer provides silicon atoms such that a titanium silicide local interconnect is formed.

10 Another aspect of the invention comprises a method of forming a local interconnect on a semiconductor integrated circuit. The method comprises forming a gate stack having at least one conductive layer and a source layer positioned on top of the at least one conductive layer, the source layer providing a source of transforming atoms. The method further comprises exhuming a first layer of the gate stack so as to expose a portion of the source layer. The method further comprises depositing a refractory metal on the integrated circuit so that the refractory metal contacts the exposed portion of the source material of the gate stack and so that the refractory metal is positioned on another device of the integrated circuit. The method further comprises transforming the refractory metal into a conductive material wherein the source material provides transforming atoms to the portion of the refractory metal positioned adjacent the exposed portion of the source material.

20 In one embodiment, the transforming atoms are comprised of silicon such that the local interconnect forms a silicide material at the exhumed contact. In this embodiment, the method of forming a local interconnect further comprises removing the excess refractory material such that the refractory silicide contact is substantially preserved. In this embodiment, the source material provides sufficient silicon atoms to the refractory material during transformation of the refractory material to reduce undercutting of the refractory silicide contact at the exposed surface of the source material.

25 From the foregoing, it should be apparent that the local interconnect of the integrated circuit of the present invention is improved over those known in the art. In particular, since the source material of the gate stack readily supplies source atoms to the refractory metal to abundantly form a silicide contact at the gate stack, the problem of undercutting at the exhumed surface of the gate stack is substantially reduced. These and

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other objects and advantages of the present invention will become more apparent from the following description taken in conjunction with the accompanying drawings.

Brief Description of the Drawings

5 Fig. 1 is a partial schematic sectional view of a conventionally formed silicide local interconnect;

 Fig. 2 is a schematic diagram of an exemplary conventional CMOS SRAM circuit; and

 Figs. 3-7 are partial schematic sectional views of the integrated circuit of the
10 present invention which schematically illustrates the method of forming an improved local interconnect.

Detailed Description of the Preferred Embodiment

 Reference will now be made to the drawings wherein like numerals refer to like
15 parts throughout. As is understood in the art, interconnects are used to interconnect various circuit components of semiconductor devices. To provide context and background, a circuit diagram of a typical integrated circuit formed on a semiconductor substrate is initially described in connection with Fig. 2. The circuit illustrated in Figure 2 is simply one example of a typical circuit formed on an integrated circuit that
20 requires the use of low resistance local interconnects. It will be appreciated from the following discussion that local interconnects are used in many different types of integrated circuits including SRAM, DRAM and other non-memory circuits and, as such, the present invention should not be limited to only the circuit of Fig. 2. The process by which the interconnect of the illustrated embodiment will be described in
25 greater detail below in connection with Figs. 3 - 7.

 As shown in Fig. 2, an exemplary SRAM device 30 comprises six CMOS transistors P1, P2, N1, N2, N3 and N4 connected together in a symmetrical configuration. In particular, the transistor P1, having a source 32, a drain 34, and a gate 36, and the transistor N1, having a source 38, a drain 40, and a gate 42, are configured such that the
30 drain region 34 of P1 couples with the source region 38 of N1 at a node X1 and such that the gate regions 36 and 42 are interconnected at a node X2. Likewise, the transistors P2

and N2 are configured in a similar manner such that the drain region of P2 couples with the source region of N2 at a node X3 and such that the gate regions interconnect at a node X4. As shown in Fig. 2, the SRAM device further comprises a local interconnect L1 and a local interconnect L2. In particular, the local interconnect L1 cross-couples the node X1 with the Node X4, whereas the local interconnect L2 cross-couples the node X2 with the node X3. Thus, the local interconnects L1 and L2 are each required to interconnect a gate electrode with an active source/drain region.

As is illustrated by this exemplary circuit, various circuit components formed in a semiconductor substrate have to be interconnected via low resistance interconnection paths. Typically, various semiconductor structures, such as the CMOS gates, are formed at different locations on a semiconductor wafer and silicide interconnects are formed so as to be electrically coupled to the semiconductor devices and thereby electrically interconnect the devices with a low resistance path. As discussed above, it is desirable that the local interconnects between devices of a circuit, such as a SRAM or DRAM circuit, have as low of resistance as possible.

Reference will now be made to Figs. 3 through 7 which illustrate a method of forming the local interconnect, such as the interconnect L1 of Fig. 1. In particular, the local interconnect is formed between an exhumed gate electrode 60 (Fig. 7) and an active source/drain region 62 of a semiconductor substrate 64. However, it will be appreciated that the method described hereinbelow could be adapted to form a similar local interconnect that couples the gate electrode with a different circuit node, such as another gate electrode.

As shown in Fig. 3, the semiconductor substrate 64, preferably formed of silicon, is prepared with isolation regions 66 using a conventional isolation process, such as local oxidation of silicon (LOCOS) or STIC shallow trench isolation. The isolation regions 66 are used to define active areas of the substrate. In these applications, the active areas will contain the source/drain regions of the transistors forming the memories.

As shown in Fig. 3, a plurality of blanket layers 52 are then deposited over the substrate 64. In particular, the blanket layers 52 comprise a blanket gate oxide layer 68, a blanket polysilicon layer 70, a blanket conductive layer 72, a blanket source layer 74, and a blanket cap insulating layer 76. Specifically, a blanket layer is defined in this

application as a substantially planar layer that extends substantially beyond the local interconnect. In one embodiment, the blanket layers 52, 68, 70, 72, 74 and 76 can cover an entire wafer of semiconductor substrate material.

5 In one embodiment, the gate oxide layer 68, preferably having a thickness between 20 Angstroms and 100 Angstroms is first deposited over the substrate 64. The gate oxide layer 68 will be patterned and etched so as to form a portion of the gate of a transistor as will be described in greater detail below.

10 Overlying the gate oxide layer 68 in this embodiment is the layer of polysilicon 70 having a thickness between 300 Angstroms and 1000 Angstroms. The polysilicon layer 70 is substantially conductive along an outward direction that is perpendicular to the plane of the polysilicon layer 70 and helps to activate the gate of the transistor. Overlying the polysilicon layer 70 is the layer 72 of conductive material, such as tungsten silicide (WSix), having a thickness between 100 Angstroms and 1000 Angstroms. The tungsten silicide layer 72 is substantially conductive along a lateral direction that is parallel to the
15 plane of the layer 72 so as to allow for better lateral transmission of current over extended regions of the integrated circuit.

Overlying the conductive layer 72 in this embodiment is the silicon-rich source layer 74, such as polysilicon, having a thickness between 100 Angstroms and 1000 Angstroms. As will be described in greater detail hereinbelow, the source layer 74
20 provides a source of transforming atoms, such as silicon atoms, during a subsequent annealing step to permit better formation of a silicide local interconnect between adjacent structures on the semiconductor surface. Overlying the silicon-rich layer 74 in this embodiment is the cap insulating layer 76 formed of either silicon oxide (SiO_2) or silicon nitride having a thickness between 1000 Angstroms and 3000 Angstroms. The cap
25 insulating layer 76 is formed, in one embodiment, using well-known oxidation techniques and acts to provide additional isolation between adjacent devices.

As shown in Fig. 4, material from the plurality of blanket layers 52 of Fig. 3 is selectively removed to form a plurality of gate stacks 78. In particular, the gate stacks 78 may be formed using conventional mask and etch technology in a well-known manner.
30 Thus, each of the gate stacks 78 comprises the gate oxide layer 68, the polysilicon layer

70, the conducting layer 72, the silicon-rich source layer 74, and the cap insulating layer 76.

As shown in Fig. 4, a portion of the cap insulating layer 76 of a gate stack 78a is then removed so as to exhume a surface of the silicon-rich layer 74, hereinbelow referred to as the exhumed surface 80. In particular, the exhumed surface 80 of Fig. 4 corresponds to the node of an integrated circuit that is to be interconnected via a local interconnection of the illustrated embodiment. The exhumed contact can, for example, comprise the node X4 of the circuit shown in Fig. 2.

As shown in Fig. 4, following the formation of the gate stacks 78 and the exhumation of the exhumed surface 80, a plurality of vertical spacers 82 are formed along the vertical edges of the gate stacks. In particular, the spacers 82 may be formed in a well-known manner of either undoped silicon dioxide or silicon nitride. Furthermore, the spacers provide electrical isolation between the exhumed surface and overlying structures of the device (not shown).

As shown in Fig. 4, the active region 62 of the substrate can also be configured using known doping techniques, such as ion implantation, so as to form a source/drain region of a MOSFET transistor. Thus, the active region 62 of Fig. 4 can, for example, correspond to the node X1 of the circuit shown in Fig. 2.

As shown in Fig. 5, a blanket refractory metal layer 84 is deposited over the intermediate structure of Fig. 4 so as to overlay the active area 62 of the substrate 64 and the exhumed surface 80 of the gate stack 78a. The refractory metal layer 84 is deposited using well-known metal deposition techniques, such as sputtering and the like. Preferably, the refractory metal is a metal that will form a low resistance silicide or nitride during a subsequent annealing step as will be described below. In one embodiment, the refractory metal layer 84 comprises titanium having a thickness between 100 Angstroms and 500 Angstroms.

As shown in Fig. 5, a masking layer 86 is deposited over the refractory metal layer 84 and subsequently etched so as to define the extent of the local interconnect. Thus, the masking layer 86 defines an exposed region 88 that extends beyond the masking layer 86 and a covered region 90 that lies underneath the masking layer 86. In one embodiment, the masking layer 86 is substantially comprised of tungsten silicide (WSix) material. In

another embodiment, the masking layer 86 is formed of a silicon material. In yet another embodiment, the masking layer 86 is formed of a polysilicon material. In still yet another embodiment, the masking layer 86 is formed of a silicon oxynitride material.

5 The intermediate structure of Fig. 5 then undergoes an annealing process such that it is exposed to a high temperature environment with an N₂/NH₃ ambient source. This preferably comprises exposing the refractory material to a rapid thermal processing environment having the N₂/NH₃ ambient so as to increase the temperature of the refractory material to a value between 600 degrees Celsius and 750 degrees Celsius for a period of time between 10 seconds and 60 seconds. In one particular embodiment, the
10 titanium refractory material is annealed by raising its temperature to a value of 710 degrees Celsius for a time period of between 20 and 30 seconds in the presence of the N₂/NH₃ ambient.

Thus, the refractory metal layer 84 is induced to react with silicon from the silicon-rich source layer 74 of the gate stack 78a to form a refractory silicide contact 92 at the
15 exhumed surface 80 of the gate stack 78a as shown in Fig. 6. Likewise, a refractory silicide contact 94 is also formed at the active region 62 of the substrate 64. Furthermore, the exposed region 88 of the refractory metal 84 which is exposed to the N₂/NH₃ ambient will form refractory nitride 96. Moreover, if the masking layer 86 is formed of polysilicon, the covered region 90 of the refractory metal 84 will combine with silicon
20 from the masking layer 86 to form a conductive layer 98 of refractory silicide that extends between the refractory silicide contacts 92 and 94. Alternatively, if the masking layer 86 is a poor source of silicon, such as tungsten silicide (WSi_x), the conductive path 98 between the refractory silicide contacts is substantially provided by the unreacted refractory metal 84 in the covered region 90.

25 The intermediate structure of Fig. 6 is then exposed to a wet etching process that removes excess refractory material and leaves behind the local interconnect 50, as shown in Fig. 7. In particular, an etchant which selectively removes refractory nitride and refractory metal material, such as H₂O:H₂O₂:NH₄OH having a ratio of 1:0.25:0.25, removes the refractory nitride 96 and unreacted refractory metal 84 of Fig. 5 from the
30 exposed region 88. Furthermore, since the etchant does not substantially remove refractory silicide material, the refractory silicide contacts 92 and 94 are substantially

unaffected by the etchant. Moreover, since the covered region 90 of the refractory metal 84 either combines with silicon from the masking layer 86 to form a refractory silicide layer 98 or is protected by the masking layer 86, the covered region 90 of the local interconnect 50 remains unaffected by the wet etching process. Thus, the resulting local interconnect 50 provides a substantially low resistance conductive path between the exhumed surface 80 of the gate stack 78a and the active region 62 of the substrate 64.

It will be appreciated that the silicide contact 92 of the interconnect 50 formed at the exhumed surface 80 of the gate stack 78a is formed with a substantially small sheet resistance. In particular, since the exhumed layer 74 of the gate stack is a rich source of silicon atoms, the refractory metal 84 will readily react to generously form refractory silicide at the exhumed surface 80. Thus, at most, only a small amount of unreacted refractory metal remains at the exhumed surface 80 and a small amount of refractory nitride is formed at the exhumed surface 80. Therefore, the wet etch process described in connection with Fig. 7 does not substantially degrade of the refractory silicide contact 92. Consequently, the problem of undercutting of the refractory silicide contact 92, which exists in the prior art, is substantially reduced.

It will also be appreciated that the method of forming the interconnect 50 is relatively simple to implement. In particular, the only extra processing step is that of depositing the silicon-rich layer 74 during the formation of the gate stacks 78. Furthermore, since the silicon-rich layer 74 is selectively etched during the same etching process that selectively etches the oxide layer 68, the polysilicon layer 70, the conducting layer 72, and the cap insulating layer 76, no additional etching process is required.

It will be appreciated that the improved process of forming the interconnect so as to reduce undercutting allows for smaller contact geometries at exhumed contacts. Undercutting at the connection between the local interconnect and the exhumed contact is a more significant problem in smaller geometry devices. Hence, by developing a technique for reducing undercutting, smaller local interconnects can be used thereby facilitating higher scales of integration.

Although the preferred embodiment of the present invention has shown, described and pointed out the fundamental novel features of the invention as applied to this embodiment, it will be understood that various omissions, substitutions and changes in the

form of the detail of the device illustrated may be made by those skilled in the art without departing from the spirit of the present invention. Consequently, the scope of the invention should not be limited to the foregoing description, but should be defined by the appended claims.